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PATENT APPLICATION

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In re Application of:	)	
	:	Examiner: L. Nguyen
MASAHIKO WATANABE	)	
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Appln. No.: 09/919,902	)	
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Filed: August 2, 2001	)	
	:	
For: INTEGRATED-CIRCUIT APPARATUS AND INK JET RECORDING APPARATUS USING THE SAME	)	
	:	August 13, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBMISSION OF SWORN TRANSLATION OF PRIORITY DOCUMENT

Sir:

Applicant is submitting herewith a sworn English translation of Japanese Patent Application No. 2000-238378 filed August 7, 2000, on which the above-identified U.S. patent application claims priority.

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Respectfully submitted,

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[Title of the Invention] Large-scale Integrated-circuit Apparatus

[Number of the Claims] 8

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[Material] Specification 1

[Material] Drawings 1

[Material] Abstract 1

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2000-238378

[Name of the Document] Specification

[Title of the Invention] Large-scale Integrated-circuit Apparatus

[What is Claimed is]

[Claim 1]

A large-scale integrated-circuit apparatus having a plurality of circuits respectively to be initialized when an electrical power source is turned on, further comprising:

first reset signal generating means disposed in a predetermined circuit out of said plurality of circuits for performing initialization of said predetermined circuit when receiving an external reset signal generated over a predetermined period of time from the start of supply of the electrical power from the outside and, at the same time, generating a first reset signal;

second reset signal generating means for generating a second reset signal when already having received said external reset signal and receiving said first reset signal from said first reset signal generating means; and

initialization means disposed in other circuit than said predetermined circuit out of said plurality of circuits for performing initialization of said other circuit when receiving said reset signal by the use of said second reset signal generating means.

[Claim 2]

A large-scale integrated-circuit apparatus

according to claim 1, wherein said predetermined circuit is a CPU (central processing unit).

[Claim 3]

A large-scale integrated-circuit apparatus according to claim 1 or 2, wherein said other circuit is a peripheral logic circuit.

[Claim 4]

A large-scale integrated-circuit apparatus according to any one of claims 1 to 3, wherein said other circuit is an application specific logic circuit.

[Claim 5]

A large-scale integrated-circuit apparatus according to claim 1 or 2, wherein said other circuit is a peripheral logic circuit and application specific logic circuit, and which apparatus further comprising:

first initialization completion signal generating means disposed in said peripheral logic circuit for generating a first initialization completion signal when initialization of said peripheral logic circuit is completed;

second initialization completion signal generating means disposed in said application specific logic circuit for generating a second initialization completion signal when initialization of said application specific logic circuit is completed; and

regenerating means disposed in said predetermined circuit for regenerating said first reset signal when at

least one of said first and second initialization completion signals is not generated.

[Claim 6]

A large-scale integrated-circuit apparatus according to any one of claims 1 to 5, wherein said large-scale integrated-circuit apparatus is constituted by one chip.

[Claim 7]

A large-scale integrated-circuit apparatus according to any one of claims 1 to 6, wherein initialization of said predetermined circuit or said other circuit is performed at a clock-synchronized timing.

[Claim 8]

A large-scale integrated-circuit apparatus according to any one of claims 1 to 7, wherein said large-scale integrated-circuit is used in a printer apparatus.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Utilization]

The present invention relates to a large-scale integrated-circuit apparatus, particularly to a large-scale integrated-circuit apparatus comprising a plurality of circuits to be initialized when an electrical power source is turned on.

[0002]

[Prior Art]

An application specific integrated circuit (hereafter referred to as ASIC) has been developed so far which is not a general-purpose IC such as a CPU or a memory but an IC for realizing a function most suitable for a specific purpose.

[0003]

Because the semiconductor-integrated-circuit art has been recently developed, the operation speed, integration degree, and scale of the ASIC of this type have been improved and moreover, each circuit constituting the ASIC has been developed from a circuit having a single function to a circuit having a multiple function.

[0004]

In the case of an ASIC, at least three types of circuits such as a CPU, an I/O exspander, and an application specific logic circuit have been independently improved in integration degree, operation speed, and scale. However, because the semiconductor-integrated-circuit art for a one-chip configuration including every function in the same chip has been recently established, further-advanced integration is realized. Also in the case of an ASIC, a CPU, an I/O expander, and an application specific logic circuit are integrated on one semiconductor wafer by the semiconductor-integrated-circuit art for realizing a one-chip configuration.

[0005]

The above semiconductor integrated circuit greatly

advanced in integration samples an external input signal in accordance with an external clock signal and captures it. Moreover, an internal circuit operates by converting an external clock signal into a sync signal.

[0006]

[Problems to be Solved by the Invention]

As described above, in the case of a conventional ASIC advanced in integration, though a plurality of circuits mounted on a semiconductor wafer respectively synchronize with an external clock signal, each circuit only independently functions. That is, though a circuit operation synchronizes with a clock, initialization (reset) operation of each circuit when an electrical power source is turned on is independently performed. Therefore, a slight difference occurs between reset timings of the circuits and this makes operations of an ASIC unstable.

[0007]

The above mentioned is described below by referring to FIG. 3 showing a block diagram of a conventional ASIC. Symbol 101 denotes an ASIC.

[0008]

Referring to FIG. 3, a CPU 102, a peripheral logic circuit 103, and an application specific logic circuit 104 are set in the ASIC 101. The peripheral logic circuit 103 controls transfer of data between a memory (not shown) built in the ASIC 101, a program ROM (not shown) set to the outside of the ASIC 101, and the application specific logic circuit

104 on one hand and the CPU 102 on the other. The application specific logic circuit 104 is a logic circuit to be set to a specific control unit on which the ASIC 101 is mounted by a user in order to optimize the ASIC 101.

[0009]

Symbol 105 denotes a clock signal supplied from an external unit to the ASIC 101, which is used to synchronize internal circuits of the ASIC 101. Symbol 106 denotes a reset signal supplied from an external unit to the ASIC 101. Symbol 108 denotes an inverter circuit set in the ASIC 101 to logic-invert the reset signal 106.

[0010]

In the case of the above conventional ASIC 101, when the reset signal 106 is input for a predetermined period in accordance with rise of an electrical power source, an internal reset signal 108 obtained by inverting the reset signal 106 is input to reset terminals of the CPU 102, peripheral logic circuit 103, and application specific logic circuit 104. The CPU 102, peripheral logic circuit 103, and application specific logic circuit 104 are initialized by receiving the internal reset signal 108.

[0011]

However, because a difference occurs between rises of voltages of the CPU 102, peripheral logic circuit 103, and application specific logic circuit 104 after start of power supply, reset timings of the circuits 102, 103, and 104 are slightly different from each other. Therefore, the

reset timing of the CPU 102 may be later than the reset timings of the peripheral logic circuit 103 and the application specific logic circuit 104, depending on a timing difference therebetween. In this case, a problem occurs that stable operations of the ASIC 101 cannot be expected.

[0012]

The present invention is made to solve the above problems and its object is to provide a large-scale integrated-circuit apparatus for controlling the reset timing of each circuit to a proper value when initializing a plurality of circuits constituting an ASIC.

[0013]

[Means for Solving the Problems]

In order to achieve the above object, according to claim 1 of the present invention, there is provided a large-scale integrated-circuit apparatus having a plurality of circuits respectively to be initialized when an electrical power source is turned on, further comprising: first reset signal generating means disposed in a predetermined circuit out of the plurality of circuits for performing initialization of the predetermined circuit when receiving an external reset signal generated over a predetermined period of time from the start of supply of the electrical power from the outside and, at the same time, generating a first reset signal; second reset signal generating means for generating a second reset signal when

already having received the external reset signal and receiving the first reset signal from the first reset signal generating means; and initialization means disposed in other circuit than the predetermined circuit out of the plurality of circuits for performing initialization of the other circuit when receiving the reset signal by the use of the second reset signal generating means.

[0014]

[Description of the Preferred Embodiments]

Embodiments of the present invention are described below by referring to the accompanying drawings.

[0015]

FIG. 1 is a block diagram showing a configuration of a first embodiment of a large-scale integrated-circuit apparatus of the present invention.

[0016]

Symbol 1 denotes an ASIC (application specific integrated circuit). Symbol 2 denotes a unit serving as a CPU set in the ASIC 1 in this embodiment. Symbol 3 denotes a unit serving as a peripheral logic circuit set in the ASIC 1 in this embodiment. The peripheral logic circuit 3 is a unit for transferring data between a memory (not shown) built in the ASIC 1, a program ROM (not shown) set to the outside of the ASIC 1, and the application specific logic circuit 4 on one hand and the CPU 2. Symbol 4 is a logic circuit to be set by the user for optimizing the ASIC 1 for a specific control device. Such a logic circuit has a scale

of approx. hundred thousands of gates.

[0017]

Symbol 5 denotes a clock signal supplied from an external unit to the ASIC 1, which is used to synchronize internal circuits of the ASIC 1. Symbol 6 denotes a reset signal supplied from an external unit to the ASIC 1, which is used to initialize the CPU 2 in the ASIC 1. Symbol 7 denotes an inverter circuit set in the ASIC 1 to logic-invert the reset signal 6. Symbol 8 denotes the inverted signal of the reset signal 6, which is an internal reset signal to be transferred to logic circuits 3 and 4 in the ASIC 1.

[0018]

Symbols 9a, 9b, and 9c denote flip-flop circuits (hereafter referred to as F/F circuits). The F/F circuit 9a is a circuit for clock-synchronizing the reset signal 6 and the F/F circuits 9b and 9c are circuits for clock-synchronizing output signals of inverting AND circuits 10a and 10b to be described later. Output signals of the F/F circuits 9a, 9b and 9c are supplied to reset terminals of the CPU2, the peripheral logic circuit 3 and application specific logic circuit 4.

[0019]

Symbols 10a and 10b denote inverting AND circuits, which compute the inverting AND between an internal reset signal 8 and a reset confirmation signal (to be described later) sent from the CPU 2 and supply the result to the F/F

circuits 9b and 9c.

[0020]

Symbol 11 denotes an initialization-completion signal output from the peripheral logic circuit 3 when initialization of the peripheral logic circuit 3 is completed. Symbol 12 denotes an initialization-completion signal output from the application specific logic circuit 4 when initialization of the application specific logic circuit 4 is completed. Symbol 13 denotes an AND (logic) circuit which obtains the logical product between the initialization-completion signals 11 and 12 and communicates the result to the CPU 2 as an initialization-completion notification signal.

[0021]

Symbols 15a and 15b denote data buses used to transfer data between the CPU2, the peripheral logic circuit 3, and the application specific logic circuit 4.

[0022]

Then, operations of the ASIC 1 having the above configuration are described below.

[0023]

First, when power is supplied from an electrical-power-source (not shown) to the ASIC 1, a reset IC (symbol 39 in FIG. 2) monitors the power-source voltage, generates the reset signal 6 to be kept at High level (hereafter referred to as H level) only for a predetermined period (e.g. 100 ms) after start of power supply, and outputs

the signal 6 to the ASIC 1.

[0024]

When the reset signal 6 is supplied from the reset IC to the ASIC 1, the F/F circuit 9a clock-synchronizes the reset signal 6. The clock-synchronized reset signal is supplied to the reset terminal of the CPU 2 and the CPU 2 is initialized. The initialized CPU2 transmits reset confirmation signals to the inverting AND circuits 10a and 10b. The CPU2 samples the level of the signal clock-synchronized by the F/F circuit 9a. When it is confirmed that the signal level reaches the reset level over the predetermined period of time, the transmission of the reset confirmation signals to the inverting AND circuits 10a and 10b is stopped.

[0025]

The reset signal 6 supplied from the reset IC is inverted by the inverter circuit 7 and supplied to the inverting AND circuits 10a and 10b as the internal reset signal 8. The inverting AND circuits 10a and 10b receive the reset confirmation signal 19 from the CPU 2 and output an H level signal to the F/F circuits 9b and 9c when the internal reset signal 8 is kept at Low level (hereafter referred to as L level), that is, the reset signal 6 is kept at H level. The F/F circuits 9b and 9c receiving the H level signals synchronize the H level signal in accordance with the clock signal 5 and supply the signal 21 to reset terminals of the peripheral logic circuit 3 and the application

specific logic circuit 4.

[0026]

As a result, initialization is performed in the peripheral logic circuit 3 and the application specific logic circuit 4, respectively. That is, the peripheral logic circuit 3 and the application specific logic circuit 4 are not initialized until receiving not only the reset signal, but also the reset confirmation signal from the CPU 2.

[0027]

When the initialization is completed in the peripheral logic circuit 3 and the application specific logic circuit 4, the initialization completion signal 11 and 12 are respectively outputted from the peripheral logic circuit 3 and the application specific logic circuit 4. The AND circuit 13 outputs an initialization completion AND signal 14 to the CPU 2 if having received both of the initialization completion signals 11 and 12.

[0028]

When the initialization completion AND signal 14 is not supplied from the AND circuit 13 to the CPU 2 within the predetermined period of time, the CPU 2 outputs the reset confirmation signal again for a certain period to attempt initialization of the peripheral logic circuit 3 and/or application specific logic circuit 4.

[0029]

Then, a case of mounting the ASIC 1 on a printer

is described below.

[0030]

FIG. 2 is a block diagram showing a configuration of a printer 31 on which the ASIC 1 is mounted.

[0031]

Referring to FIG. 2, symbol 32 denotes a wiring board on which an electric circuit for driving the printer 31 is mounted. The ASIC 1 is mounted on the wiring board 32. Symbol 33 denotes an electrical-power-source unit that supplies power to the electric circuit on the wiring board 32 and driving units (not shown) through the electric circuit. Symbol 34 denotes an AC cable for supplying commercial power to the electrical-power-source unit 33. Symbol 35 denotes an operation-panel unit that is used for a user to operate the printer 31. Symbol 36 denotes a memory unit mounted on the wiring board 32, which temporarily stores information sent from the ASIC 1 and supplies the stored information to the ASIC 1. Symbol 37 denotes a driving circuit for controlling operations of driving parts (not shown) in the printer 31. Symbol 38 denotes an I/F connector. The printer 31 receives print data from a host computer 46 serving as an external unit of the printer 31 through the I/F connector 38. Moreover, the printer 31 supplies the set information of the printer 31, etc., to the host computer 46 through the I/F connector.

[0032]

Symbol 39 denotes a reset IC which monitors a

power-source voltage supplied from the electrical-power-source unit 33 and outputs the reset signal 6 to be kept H level for a predetermined period (e.g. 100 ms) after power supply is started. The predetermined period is set to a period necessary for internal circuits of the ASIC 1 to reach a sufficiently operable state.

[0033]

Symbol 40 denotes a clock generation circuit that generates the clock signal 5 for operating the ASIC 1 at a predetermined time interval.

[0034]

Symbol 41 denotes an operation bus disposed between the operation panel unit 35 and the ASIC 1, which sends the information supplied from the operation panel unit 35 to the ASIC 1. Moreover, the information supplied from the ASIC 1 is displayed on the operation panel unit 35. Symbol 42 denotes a memory bus disposed between the memory unit 36 and the ASIC 1, which writes the information supplied from the ASIC 1 in the memory unit 36 and reads information from the memory unit 36 to the ASIC 1. Symbol 43 denotes a DC line disposed between the electrical-power-source unit 33 and the ASIC 1 to supply DC power. The DC line 43 includes a logic-circuit power-source line for operating the ASIC 1 and the like and a driving-circuit power-source line for operating the driving circuit 37. The voltage of the driving-circuit power-source line is higher than that of the logic-circuit power-source line. Symbol 44 denotes a

driving bus for connecting the ASIC 1 with the driving circuit 37, which transfers a driving signal from the ASIC 1 to the driving circuit 37. Symbol 45 denotes an I/F bus disposed between the ASIC 1 and the I/F connector 38, which transfers the print data generated by the host computer 46 to the ASIC 1 and the information supplied from the printer 31 to the host computer 46. Symbol 47 denotes an I/F cable for transferring print data from the host computer 46 to the printer 31.

[0035]

Then, operations of the printer 31 are described below.

[0036]

The printer 31 is operated by inserting the AC cable 34 into a commercial-power-source outlet. First, by inserting the AC cable 34 into the outlet, the power-source unit 33 converts AC (commercial power) into a DC power-source voltage (logic-circuit power-source voltage and driving-circuit power-source voltage) used for the printer 31 and outputs the voltage to the DC line 43. The DC line 43 is connected to the ASIC 1 and reset IC 39 to drive the ASIC 1 and reset IC 39. In this case, the reset IC 39 always monitors the supply voltage of the DC line 43 and when detecting that power is supplied, it outputs the reset signal 6 to be kept H level for a predetermined period (e.g. 100 ms) after detecting that the power is supplied to the ASIC 1. The above predetermined period is set to a period

necessary for internal circuits of the ASIC 1 to reach a sufficiently operable state.

[0037]

Operations of the ASIC 1 to which the reset signal 6 is supplied are performed as described for FIG. 1.

[0038]

[Effect of the Invention]

As described above, according to the present invention, in a large-scale integrated-circuit apparatus having a plurality of circuits respectively to be initialized when an electrical power source is turned on, a predetermined circuit out of the plurality of circuits performs, when receiving an external reset signal generated over a predetermined period of time from the start of supply of the electrical power from the outside, initialization of the predetermined circuit and, at the same time, generates a first reset signal. Also, when the external reset signal is inputted and the first reset signal is generated, a second reset signal is generated. Then, other circuit than the above predetermined circuit, out of the plurality of circuits, performs initialization of the other circuit when receiving the second reset signal.

[0039]

With this arrangement, the predetermined circuit completing the initialization controls the initialization of the other circuit so as to control a timing of the initialization properly. Consequently it is possible to

prevent inappropriate lag of timing of initialization among the plurality of circuits mounted on the large-scale integrated-circuit apparatus, so as to remove instability of operation generated in the large-scale integrated-circuit apparatus.

[Brief Description of the Drawings]

[Figure 1]

A block diagram showing a configuration of a large-scale integrated-circuit apparatus according to the first embodiment of the present invention.

[Figure 2]

A block diagram showing a configuration of a printer having an ASIC 1.

[Figure 3]

A block diagram showing a configuration of a conventional ASIC.

[Description of Reference Numerals or Symbols]

1 … ASIC (large-scale integrated-circuit apparatus)

2 … CPU (predetermined circuit, first reset signal generating means)

3 … peripheral logic circuit (other circuit, initialization means)

4 … application specific circuit (other circuit, initialization means)

5 … clock signal

6 … reset signal (external reset signal)

7 … inverter circuit

8 … internal reset signal

9a, 9b, 9c … F/F circuits

10a, 10b … inverting AND circuits (second reset signal generating means)

11 … initialization completion signal

12 … initialization completion signal

13 … AND circuit

14 … initialization completion AND signal

10a, 10b … data buses

31 … printer apparatus

32 … wiring board

33 … electrical-power-source unit

34 … AC cable

35 … operation-panel unit

36 … memory unit

37 … driving circuit

38 … I/F connector

39 … reset IC

40 … clock generation circuit

41 … operation bus

42 … memory bus

43 … DC line

44 … driving bus

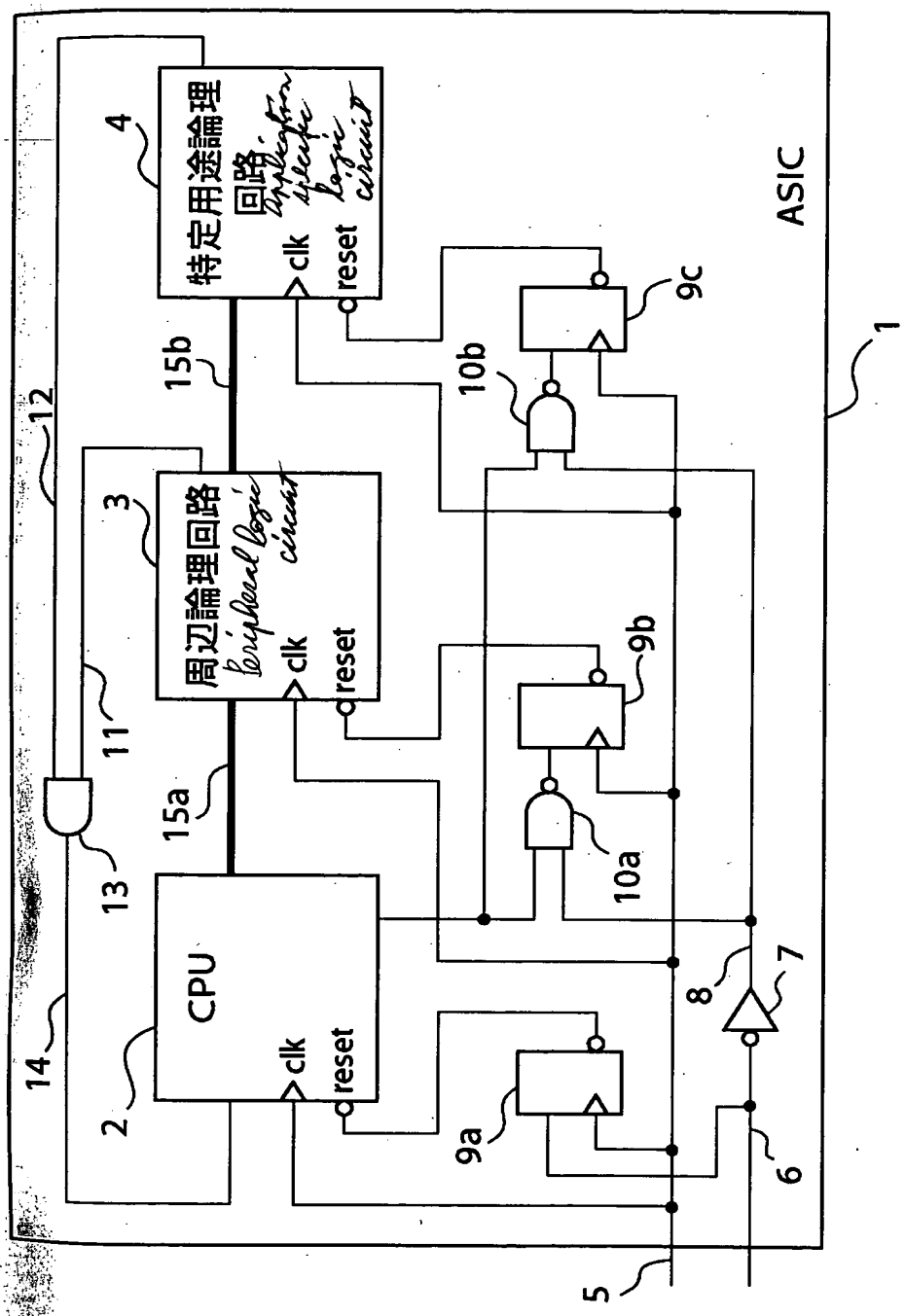
45 … I/F bus

46 … host computer

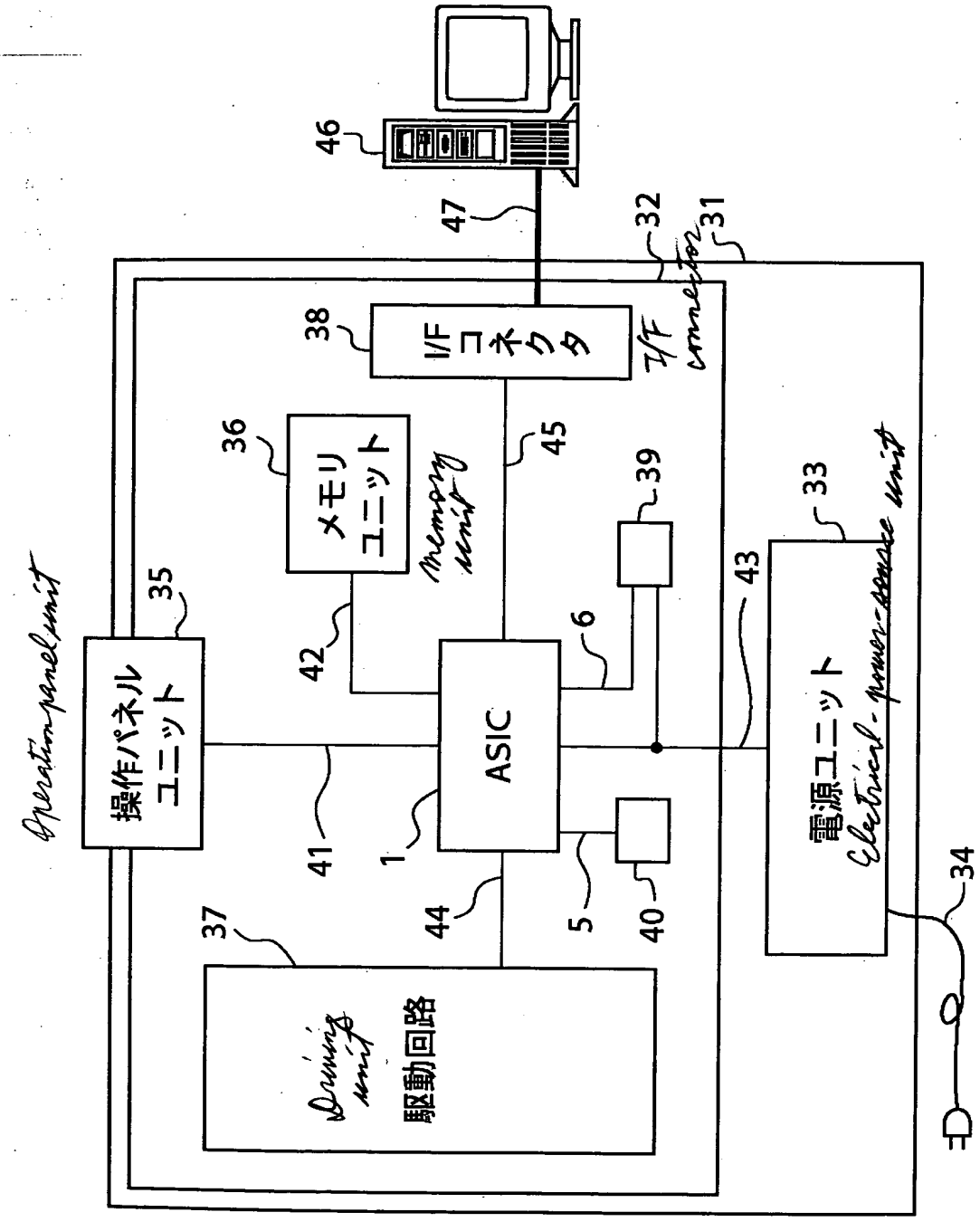
47 … I/F cable

【書類名】　図面　〔Name of the Document〕 Drawings

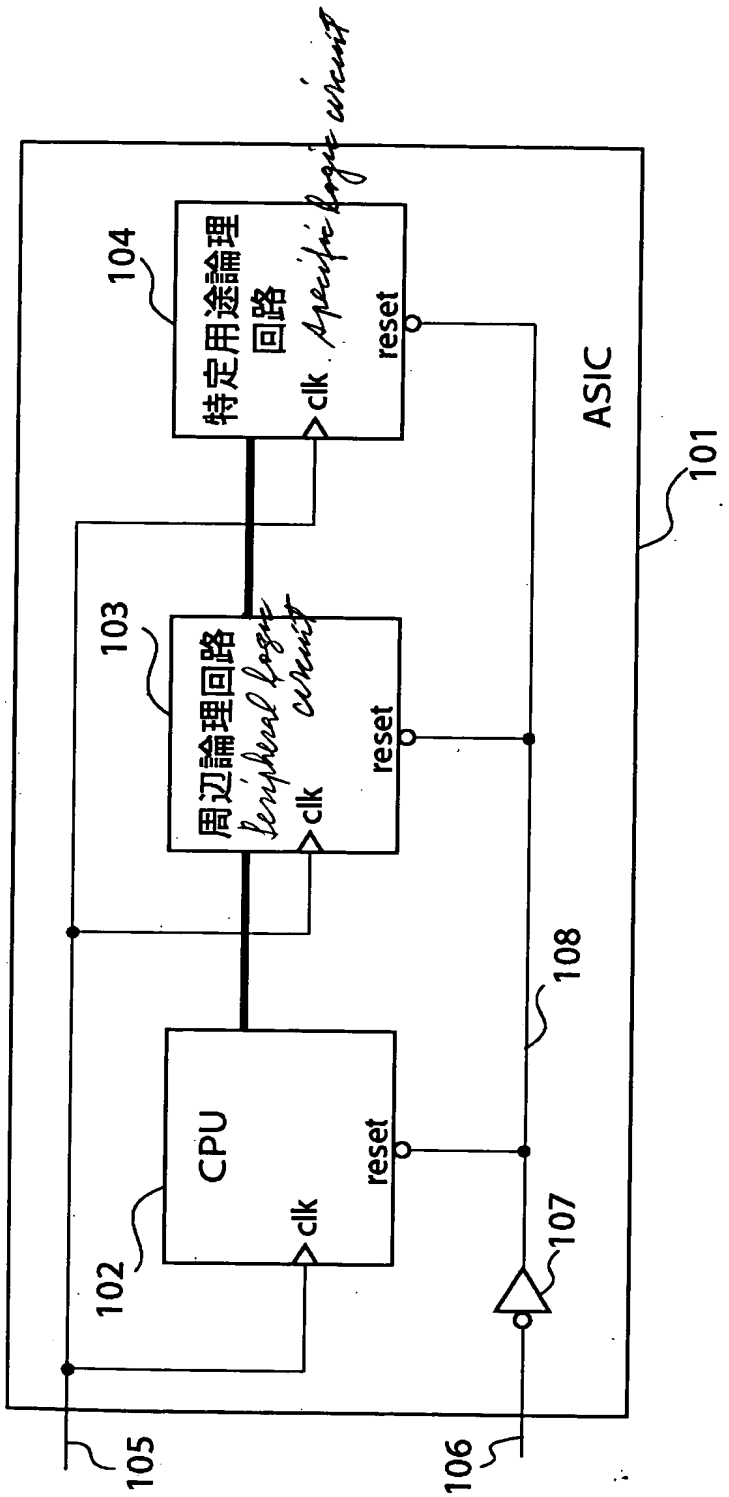
【図１】 Fig. 1



【図２】 Fig. 2


46
47
32
31
38
I/F コネクタ
I/F connector
36
メモリユニット
memory unit
45
39
33
43
Operation panel unit
35
操作パネルユニット
42
6
電源ユニット
Electrical power source unit
41
1
ASIC
44
5
40
34
37
Driving unit
駆動回路

【図３】 Fig 3


ASIC
101
特定用途論理回路
Specific logic circuit
104
clk
reset
周辺論理回路
peripheral logic circuit
103
clk
reset
CPU
102
clk
reset
108
107
105
106

[Name of the Document] Abstract

[Abstract]

[Object]

An object of the present invention is to control the reset timing of each circuit to a proper value when initializing a plurality of circuits constituting an ASIC.

[Means for Achieving the Object]

In an ASIC (Application Specific Integrated Circuit) having a CPU 2, a peripheral logic circuit 3 and an application specific logic circuit 4, when the CPU 2 receives an external reset signal 6 which is generated over a predetermined period from the start of the power supply from the outside, the initialization of the CPU 2 is performed and, at the same time, a first reset signal is generated. The inverting AND circuits 10a and 10b have already received an inverted signal 8 of the external reset signal, and when receiving the first reset signal, a second reset signal is generated. The peripheral logic circuit 3 and the application specific logic circuit 4 perform, when receiving the second reset signal, initialization of its own.

[Elected Drawing]

Figure 1

Applicant's Information

Identification No.		[000001007]
1.	Date of Change	August 30, 1990
	[Reason for Change]	New Registration
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